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(54) Title: METHOD, CIRCUIT AND SYSTEMS FOR ERASING ONE OR MORE NON-VOLATILE MEMORY CELLS

(57) Abstract: The present invention is a method circuit and system for erasing one or more non-volatile memory ("NVM") cells in an NVM array. One or more NVM cells of a memory array may be erased using an erase pulse produced by a controller and/or erase pulse source adapted to induce and/or invoke a substantially stable channel current in the one or more NVM cells during an erasure procedure. The voltage profile of an erase pulse may be predefined or the voltage profile of the erase pulse may be dynamically adjusted based on feedback from a current sensor during an erase procedure.

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METHOD, CIRCUIT AND SYSTEMS FOR ERASING ONE OR MORE NON-VOLATILE MEMORY CELLS

FIELD OF THE INVENTION

[0001] The present invention generally relates to the field of non-volatile memory ("NVM") cells. More specifically, the present invention relates to a method, circuit and system for erasing one or more NVM cells using one or more non-constant voltage erase pulses.

BACKGROUND OF THE INVENTION

[0002] Non-volatile memory ("NVM") cells are fabricated in a large variety of structures, including but not limited to Poly-silicon floating gate, as shown in FIG. 2A, and Nitride Read Only Memory ("NROM"), as shown in FIG. 2B. As is well known, an NVM cell's state may be defined and determined by its threshold voltage ("Vt"), the gate to source/drain voltage at which the cell begins to significantly conduct current.

[0003] Different threshold voltage ranges are associated with different logical states, and a NVM cell's threshold voltage level may be correlated to the amount of charge (e.g. electrons) stored in a charge storage region of the cell. Fig. 1A shows a voltage distribution graph depicting possible threshold voltage distributions of a binary non-volatile memory cell, wherein vertical lines depict boundary voltage values correlated with each of the cell's possible states. Cells having Vt Lower than EV level may be said to be erased verified. Cells having Vt Higher than PV may be said to be program verified. These two limits define the completion of programming and erase sequences that may be performed on a cell. A Program sequence of programming pulses may be used to drive the Vt of a cell higher than PV, while an erase sequence may drive the cell's Vt lower than EV. Also visible in Fig. 1A are vertical lines designating a Read Verify (RV) level and an Intermediate Program Verify voltage, PV^I, designating the start of regions before the Program Verify threshold.

[0004] FIG 1B shows a voltage distribution graph depicting possible threshold voltage distributions in the charge storage region of a multi-level non-volatile memory cell ("MLC"), wherein one set of vertical lines depict boundary values correlated with each of the cell's possible Program Verify Threshold Voltages (PV00, PV01, etc.), another set of vertical lines depict boundary values correlated with the Read Verify level of each of the cell's possible Program states (RV00, RV01, etc.), and yet another set depict boundary lines for Intermediate Program Verify voltages (PV'00, PV'01, etc..) associated with each of the states.

[0005] The amount of charge stored in a charge storage region of an NVM cell, may be increased by applying one or more programming pulses to the cell. While the amount of charge in the cell may decrease by applying an erase pulse to the NVM cell which may force the charge reduction in the cell's charge storage region, and consequently may decrease the NVM's threshold voltage.

[0006] A simple method used for operating NVM cells (e.g. programming, reading, and erasing) uses one or more reference structures such as reference cells to generate the reference levels (i.e. PVs, EVs). Each of the one or more reference structures may be compared against a memory cell being operated in order to determine a condition or state of the memory cell being operated. Generally, in order to determine whether an NVM cell is at a specific state, for example erased, programmed, or programmed at one of multiple possible program states within a multi-level cell ("MLC"), the cell's threshold level is compared to that of a reference structure whose threshold level is preset and known to be at a voltage level associated with the specific state being tested for. Comparing the threshold voltage of an NVM cell to that of a reference cell is often accomplished using a sense amplifier. Various techniques for comparing an NVM's threshold voltage against those of one or more reference cells, in order to determine the state(s) of the NVM's cells, are well known.

[0007] When programming an NVM cell to a desired state, a reference cell with a threshold voltage set at a voltage level defined as a "program verify" level for the given state may be compared to the threshold voltage of the cell

being programmed in order to determine whether a charge storage area or region of the cell being programmed has been sufficiently charged so as to be considered "programmed" at the desired state. If after a programming pulse has been applied to a cell, it has been determined that a cell has not been sufficiently charged in order for its threshold voltage to be at or above a "program verify" level (i.e. the threshold voltage of the relevant reference cell) associated with the target program state, the cell is typically hit with another programming pulse to try to inject more charge into its charge storage region. Once a cell's threshold value reaches or exceeds the "program verify" level to which it is being programmed, no further programming pulse should be applied to the cell.

[0008] Groups or sets of cells within an NVM array may be programmed and/or erased concurrently. The group or set of NVM cells may consist of cells being programmed to (or erased from) the same logical state, or may consist of cells being programmed to (or erased from) each of several possible states, such as may be the case with MLC arrays. Since not all cells have the same susceptibility to being programmed and/or being erased, cells within a set of cells receiving programming or erasing pulses may not program or erase at the same rate. Some cells may reach a target program state, or an erased state, before other cells in the same set of cells that are receiving programming or erasing pulses concurrently.

[0009] A further issue associated with the erasure of one or more NVM cells within a set of cells being erased, is that channel current invoked during NVM (e.g. NROM) cell erasure using constant voltages pulses is characterized by a high peak, which quickly subsides (See FIG. 3). The cause of such a channel current profile is carriers created by band-to-band tunneling at the surface of the deeply depleted drain junction (associated with Gate Induce Drain Leakage). More specifically, in a NVM cell, including but not limited to NROM cells, carries may be injected into the gate dielectric stack (or floating gate, if such exists), thereby reducing the vertical electric field which facilitates current flow and causing the current to subside, as evident from the current graph of FIG. 3.

[0010] One of the drawbacks of such a channel current profile during erasure is that the channel current peak in each of the NVM cells being erased limits the amount of cells that can be erased simultaneously, either due to current consumption limits imposed on memory product and/or due to limitations on the circuits implemented in the NVM product (e.g. charge pump failures). Furthermore, the efficiency of the constant voltage erase pulse also subsides with time, as is evident from the graphs in FIG. 4, which FIG. 4 shows the reduction of channel current, along with the reduction of the highest threshold voltage, within an NVM array population receiving a 3ms constant voltage erase pulse as a function of time. As evident from FIG. 4, both the channel current and the rate of the downward threshold voltage shift subsides shortly after the beginning of the erasure pulse and the erasure process becomes significantly less efficient during the latter portion of the pulse (i.e. current continues flowing ~0.4mA in this example, yet the threshold voltage downward shift is very slow).

[0011] Although during the second half of a constant voltage erase pulse a current may still flow through the cells, erasure of the cells becomes very slow and weak. Thus, the result of a channel current profile associated with a constant voltage erase pulse is; (1) relatively large current consumption during cell erasure, and (2) erasure inefficiency. These two drawbacks translate into reduced erase rates in many NVM (e.g. NROM) memory product (or any other memory technology incorporating tunnel assisted hot carrier injection), also reducing the number of cells which can be erased simultaneously and requiring that the duration of erase pulses be sufficiently long to compensate for erasure inefficiency. By comparison, whereas a typical programming pulse may have a duration of several hundred nanoseconds, a typical erase pulse may have a duration of several microseconds.

[0012] There is a need in the field of NVM production for improved methods, circuits and systems of erasing one or more NVM cells.

SUMMARY OF THE INVENTION

[0013] The present invention is a method circuit and system for erasing one or more non-volatile memory ("NVM") cells in an NVM array. According to some embodiments of the present invention, one or more NVM cells of a memory array may be erased using a controller and/or erase pulse source adapted to induce and/or invoke a substantially stable channel current in the one or more NVM cells during an erasure procedure. According to some embodiments of the present invention, the substantially stable channel current induced by the controller and/or erase pulse source may be a substantially constant channel current.

[0014] According to some embodiments of the present invention, the controller and/or erase pulse source may produce an erase pulse having a non-constant voltage profile. The erase pulse may be at a relatively smaller voltage level at its start and may grow to a relatively larger voltage level near its end. An erase pulse according to some further embodiments of the present invention may have a substantially ramp-like, trapezoidal, exponential-growth-like, or asymptote-like voltage profile, or the erase pulse may be comprised of voltage steps.

[0015] According to some embodiments of the present invention, the voltage profile of an erase pulse may be predefined, while according to other embodiments of the present invention, the voltage profile of the erase pulse may be dynamically adjusted during an erase procedure. Further embodiments of the present invention may include a current sensing circuit to sense the amount of current passing through the channels of one or more NVM cells during an erase procedure as result of an erase pulse being applied to the one or more NVM cells. A controller may receive a signal from the current sensing circuit indicating the amount of current flowing through the one or more NVM cells and may cause an erase pulse source to adjust the voltage of the current pulse being applied to the one or more NVM cells so as to maintain a substantially stable and/or substantially constant channel current through the one or more NVM cells.

[0016] According to further embodiments of the present invention, an erase pulse may be applied to sub-groups or sub-sets of a set of NVM cells to be erased in a staggered sequence. During the course of a signal erase pulse of a fixed duration, the pulse may first be applied to a first sub-set of cells. After some fraction of the fixed erase pulse duration, the pulse may than be applied to a second sub-set. A cell select and masking circuit, coupled with a controller, may facilitate a single erase pulse being applied in a staggered sequence across several sub-sets of a set of NVM cells to be erased by the given erase pulse. For example, during the first microsecond of a four microsecond erase pulse, the select circuit may only apply the erase pulse to a first sub-set of cells. After the first microsecond, the select circuit may close a switch by which the erase pulse is also applied to a second sub-set, and so on. According to some embodiments of the present invention, a circuit connecting the erase pulse to the first sub-set of NVM cells to experience the erase pulse may be opened while other sub-sets are still experiencing the erase pulse.

[0017] According to further embodiments of the present invention, a cell select and masking circuit, coupled with a controller which is receiving a signal from a current sensor, may facilitate a single erase pulse being applied in a staggered sequence across several sub-sets of a set of NVM cells to be erased by the given erase pulse. The erase pulse may first be applied to a first sub-set of cells, and once the controller receives a signal from the sensor that the current to the erase first sub-set of cells is subsiding, the controller may signal the cell select circuit to apply the erase pulse to a second sub-set. The current select circuit may apply the erase current to each additional sub-set of cells every-time the erase pulse current begins to subside and/or falls below some predefined current level, until all the sub-sets of cells have experienced the erase pulse.

[0018] The voltage of an erase pulse, according to some embodiments of the present invention, may be ramped from a low value to a desired voltage level. For example, the gates of the NVM cells to be erased may be fully biased to the desired level(s), the NVM cells' well may be grounded, the NVM cells' source lines may be floated after grounding, and the NVM cells' drain lines

may be incrementally ramped to the desired level. The NVM cells' current consumption may be continuously monitored and the voltage ramp rate may be dynamically adjusted by a feedback loop in order to prevent the current from exceeding a pre-specified limit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features and advantages thereof, may best be understood by reference to the following non limiting detailed description when read with the accompanied drawings in which:

[0020] FIG. 1A shows a voltage distribution graph depicting possible threshold voltage distributions in the charge storage region of a binary non-volatile memory cell, wherein vertical lines depict boundary values or voltage threshold level correlated with the Program Verify, Read Verify and Intermediate Program Verify levels for each of the cell's possible program states;

[0021] FIG. 1B shows a voltage distribution graph depicting possible threshold voltage distributions in the charge storage region of a multi-level non-volatile memory cell ("MLC"), wherein sets of vertical lines depict boundary values or voltage threshold levels correlated with the Program Verify, Read Verify and Intermediate Program Verify levels for each of the cell's possible states;

[0022] FIG. 2A shows a block diagram depicting a side cross sectional view of a floating gate memory cell;

[0023] FIG. 2B shows a block diagram depicting a side cross sectional view of a Nitride Read Only Memory ("NROM") cell having to distinct programming charge storage regions;

[0024] FIG. 3 is a channel current vs. time graph showing a channel current profile of an NVM cell during erasure;

[0025] FIG. 4 shows the reduction of channel current, along with the reduction of the highest threshold voltage, within an NVM array population receiving a 3ms constant voltage erase pulse as a function of time and at various erase pulse voltages;

[0026] FIG. 5 is a block diagram showing an exemplary NVM array erasing circuit according to some embodiments of the present invention;

[0027] FIG. 6 is a flow diagram of an exemplary method by which the voltage of an erase pulse according to some embodiments of the present invention may be dynamically adjusted based on feedback from a current sensor;

[0028] FIGS. 7A to 7F is a series of voltage graphs, each showing possible erase pulse voltage profiles according to various embodiments of the present invention, wherein FIG. 7F shows a voltage profile of an erase pulse dynamically stepped and adjusted based on feedback from a current sensor;

[0029] FIG. 8 is a channel current vs. time graph showing an exemplary channel current profile of an NVM cell during an erasure procedure according one or more embodiments of the present invention;

[0030] FIG. 9 is a block diagram showing another exemplary NVM array erasing circuit according to some embodiments of the present invention, including an erase pulse staggering circuit; and

[0031] FIG. 10 is a set of current graphs showing the results of staggering the application of an erase pulse to several sub-sets of a set of NVM cells, in accordance with some embodiments of the present invention.

[0032] It will be appreciated that for simplicity and clarity of these non-limiting illustrations, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION OF THE INVENTION

[0033] In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However it will be understood by those of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods and procedures have not been described in detail so as not to obscure the present invention.

[0034] Unless specifically stated otherwise, as apparent from the following discussions, it is appreciated that throughout the specification discussions utilizing terms such as "processing", "computing", "calculating", "determining", or the like, refer to the action and/or processes of a computer or computing system, or similar electronic computing device, that manipulate and/or transform data represented as physical, such as electronic, quantities within the computing system's registers and/or memories into other data similarly represented as physical quantities within the computing system's memories, registers or other such information storage, transmission or display devices.

[0035] Embodiments of the present invention may include apparatuses for performing the operations herein. This apparatus may be specially constructed for the desired purposes, or it may comprise a general purpose computer selectively activated or reconfigured by a computer program stored in the computer.

[0036] The present invention is a method circuit and system for erasing one or more non-volatile memory ("NVM") cells in an NVM array. According to some embodiments of the present invention, one or more NVM cells of a memory array may be erased using a controller and/or erase pulse source adapted to induce and/or invoke a substantially stable channel current in the one or more NVM cells during an erasure procedure. According to some embodiments of the present invention, the substantially stable channel current induced by the controller and/or erase pulse source may be a substantially constant channel current.

[0037] According to some embodiments of the present invention, the controller and/or erase pulse source may produce an erase pulse having a non-constant

voltage profile. The erase pulse may be at a relatively smaller voltage level at its start and may grow to a relatively larger voltage level near its end. An erase pulse according to some further embodiments of the present invention may have a substantially ramp-like, trapezoidal, exponential-growth-like, or asymptote-like voltage profile, or the erase pulse may be comprised of voltage steps.

[0038] According to some embodiments of the present invention, the voltage profile of an erase pulse may be predefined, while according to other embodiments of the present invention, the voltage profile of the erase pulse may be dynamically adjusted during an erase procedure. Further embodiments of the present invention may include a current sensing circuit to sense the amount of current passing through the channels of one or more NVM cells during an erase procedure as result of an erase pulse being applied to the one or more NVM cells. A controller may receive a signal from the current sensing circuit indicating the amount of current flowing through the one or more NVM cells and may cause an erase pulse source to adjust the voltage of the current pulse being applied to the one or more NVM cells so as to maintain a substantially stable and/or substantially constant channel current through the one or more NVM cells.

[0039] According to further embodiments of the present invention, an erase pulse may be applied to sub-groups or sub-sets of a set of NVM cells to be erased in a staggered sequence. During the course of a signal erase pulse of a fixed duration, the pulse may first be applied to a first sub-set of cells. After some fraction of the fixed erase pulse duration, the pulse may than be applied to a second sub-set. A cell select and masking circuit, coupled with a controller, may facilitate a single erase pulse being applied in a staggered sequence across several sub-sets of a set of NVM cells to be erased by the given erase pulse. For example, during the first microsecond of a four microsecond erase pulse, the select circuit may only apply the erase pulse to a first sub-set of cells. After the first microsecond, the select circuit may close a switch by which the erase pulse is also applied to a second sub-set, and so on. According to some embodiments of the present invention, a circuit connecting the erase pulse to the first sub-set of NVM cells to experience the

erase pulse may be opened while other sub-sets are still experiencing the erase pulse.

[0040] The voltage of an erase pulse, according to some embodiments of the present invention, may be ramped from a low value to a desired voltage level. For example, the gates of the NVM cells to be erased may be fully biased to the desired level(s), the NVM cells' well may be grounded, the NVM cells' source lines may be floated after grounding, and the NVM cells' drain lines may be incrementally ramped to the desired level. The NVM cells' current consumption may be continuously monitored and the voltage ramp rate may be dynamically adjusted by a feedback loop in order to prevent the current from exceeding a pre-specified limit.

[0041] Turing now to FIG. 5, there is shown a block diagram of an exemplary NVM array erasing circuit according to some embodiments of the present invention. An erase pulse source 110 may include a charge-pump 115, and in response to a signal from a controller 100 may produce an erase pulse with a substantially non-constant voltage profile. The controller 100 may cause the erase pulse source 110 to produce a pulse having a predefined voltage profile, for example; a ramp-like, trapezoidal, exponential-growth-like, or asymptote-like voltage profile, as shown in FIGS. 7A through 7D. According to some embodiments of the present invention, the controller 100 may cause the erase pulse source 110 to produce a pulse with a stepped voltage profile, such as those shown in FIGS. 7E through 7F.

[0042] According to further embodiments of the present invention, controller 100 may cause the erase pulse source to step the voltage of the erase pulse up and/or down in response to a signal received from a sensor 120. The sensor 120 may be a current sensor, a voltage sensor, a voltage derivative sensor or a current derivative sensor, and may provide the controller 100 a signal indicating some characteristic of the current (e.g. amount) flowing through the set of NVM cells 200 receiving the erase pulse. The controller 100 may cause the erase pulse source to adjust the voltage of an erase up or down in order to maintain a substantially stable channel current through one or more NVM cells within the set of NVM cells 200 receiving the erase pulse. For example, if either the current flowing through the channel is approaching

or exceeding some predefined current limit, of if the current is increasing very rapidly (i.e. spiking), the controller 100 may direct the pulse source 110 to step down the voltage of the erase pulse, as exemplified in the middle portion of FIG. 7F.

[0043] Turning now to FIG. 6, there is shown a flow diagram of an exemplary method/algorithm by which the voltage of an erase pulse according to some embodiments of the present invention may be dynamically adjusted based on feedback from a current sensor 120. The figure shows a specific example relating to a gate stepping based erase algorithm with real time current sensing feedback loop and adapted to maintain a constant current flowing through NVM cells experiencing an erased pulse according to some embodiments of the present invention. This algorithm may be implemented by the controller 100 or by any functionally similar circuit. It should be understood by one of ordinary skill in the art that any one of many algorithms may be used in order to maintain a substantially stable and/or substantially constant channel current through NVM cells receiving an erase pulse according to various embodiments of the present invention. FIG. 8 is a channel current vs. time graph showing an exemplary channel current profile of an NVM cell during an erasure procedure according one or more embodiments of the present invention. As evident from FIG. 8, the channel current flowing through one or more NVM cells in response to an erase pulse according to some embodiments of the present invention is substantially stable and/or constant as compared to the channel current flowing through the same one or more NVM cells in response to constant erase pulse.

[0044] Turning now to FIG. 9, there is shown a block diagram of another exemplary NVM array erasing circuit according to some embodiments of the present invention, including an NVM select and/or mark circuit 130 and an erase pulse staggering circuit 132. According to some embodiments of the present invention, an erase pulse may be applied to sub-groups or sub-sets of a set of NVM cells 200 to be erased in a staggered sequence. During the course of a signal erase pulse of a fixed duration (e.g. 3 microseconds), the pulse may first be applied to a first sub-set of cells. After some fraction of the fixed erase pulse duration, the pulse may than be applied to a second sub-set.

The cell select and masking circuit 130, coupled with the pulse staggering circuit 132 (i.e. a series of switches), may facilitate a single erase pulse being applied in a staggered sequence across several sub-sets of a set of NVM cells to be erased by the given erase pulse. For example, during the first microsecond of a four microsecond erase pulse, the select circuit may only apply the erase pulse to a first sub-set of cells. After the first microsecond, the select circuit may close a switch by which the erase pulse is also applied to a second sub-set, and so on, and so on. According to some embodiments of the present invention, a circuit connecting the erase pulse to the first sub-set of NVM cells to experience the erase pulse may be opened while other sub-sets are still experiencing the erase pulse, such that each sub-set of NVM cells experiences the erase pulse for substantially the same period of time.

[0045] According to further embodiments of the present invention, a cell select and masking circuit 130, coupled with a controller 100 which is receiving a signal from a current sensor 120, may facilitate a single erase pulse being applied in a staggered sequence across several sub-sets of a set of NVM cells 200 to be erased by the given erase pulse. The erase pulse may first be applied to a first sub-set of cells, and once the controller 100 receives a signal from the sensor 120 that the current to the erase first sub-set of cells is subsiding, the controller 100 may signal the cell select circuit 130 to apply the erase pulse to a second sub-set. The current select circuit 130 may apply the erase current to each additional sub-set of cells every-time the erase pulse current begins to subside and/or falls below some predefined current level, until all the sub-sets of cells have experienced the erase pulse.

[0046] Turning now to FIG. 10, there is shown a set of current graphs exemplifying the results of staggering the application of an erase pulse to several sub-sets of a set of NVM cells 200, in accordance with some embodiments of the present invention, such as the one shown in FIG. 9. Evident from FIG. 10, is that by applying an erase pulse to a sub-set of cells produces a lower overall peak current than applying the same erase pulse to the full set. By applying the erase pulse to each of the sub-sets in a staggered sequence (i.e. starting with the first sub-set and adding sub-sets, one sub-set at a time, each over some time interval), the overall current peak

experienced by the NVM cell array 200 may be reduced and may spread across the duration of the erase pulse.

[0047] While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

CLAIMS

What is claimed:

1. A method of erasing one or more non-volatile memory ("NVM") cells comprising:

applying to the one or more NVM cells an erase pulse having a substantially non-constant voltage profile.

2. The method according to claim 1, wherein the voltage profile of the erase pulse is predefined.

3. The method according to claim 2, wherein the erase pulse has a voltage profile selected from the group consisting of ramp-like, trapezoidal, exponential-growth-like, asymptote-like and stepped.

4. The method according to claim 3, wherein the erase pulse is applied to each sub-set of a set of NVM cells in a staggered sequence.

5. The method according to claim 1, wherein the voltage profile of the erase pulse is dynamically adjusted based on feedback.

6. The method according to claim 5, wherein the feedback comes from a sensor selected from the group consisting of a current sensor, a voltage sensor, a current derivative sensor, and a voltage derivative sensor.

7. The method according to claim 6, wherein the voltage of the erase pulse is adjusted in an inverse relation to current measure by the current sensor.

8. The method according to claim 6, wherein the voltage of the erase pulse is adjusted at a rate correlated to a signal produced by the current derivative sensor.

9. A circuit for erasing one or non-volatile memory ("NVM") cells comprising: an erase pulse source to produce an erase pulse having a substantially non-constant voltage profile.

10. The circuit according to claim 9, wherein said erase pulse source comprises a charge-pump.

11. The circuit according to claim 10, wherein the erase pulse source is adapted to produce an erase pulse having a voltage profile selected from the group consisting of ramp-like, trapezoidal, exponential-growth-like, asymptote-like and stepped.

12. The circuit according to claim 9, further comprising a cell select circuit adapted to select to which cells of a set of NVM cells the erase pulse is applied.

13. The circuit according to claim 12, wherein said cell select circuit is adapted to apply the erase pulse to each sub-set of the set of NVM cells in a staggered sequence.

14. The circuit according to claim 9, further comprising a sensor to sense a characteristic of the erase pulse as it is being applied to the one or more NVM cells.

15. The circuit according to claim 14, wherein the sensor is selected from the group consisting of a current sensor, a voltage sensor, a current derivative sensor, and a voltage derivative sensor.

16. The circuit according to claim 15, further comprising a controller to cause the erase pulse source to adjust the voltage profile of the erase pulse based on a signal from said sensor.

17. The circuit according to claim 16, wherein said controller causes the voltage of the erase pulse to be adjusted in an inverse relation to current measure by the current sensor.

18. The circuit according to claim 16, wherein said controller causes the voltage of the erase pulse to be adjusted at a rate correlated to a signal produced by the current derivative sensor.

19. A system for erasing one or non-volatile memory ("NVM") cells comprising:

A NVM array; and

an erase pulse source to produce an erase pulse having a substantially non-constant voltage profile

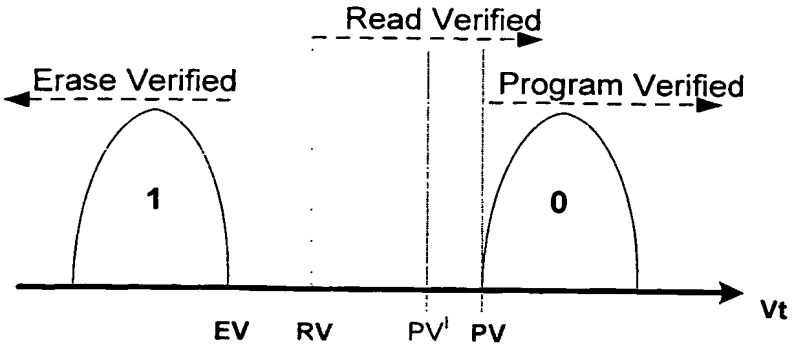

Read Verified
Erase Verified
Program Verified
1
0
Vt
EV
RV
PV'
PV

FIG 1A

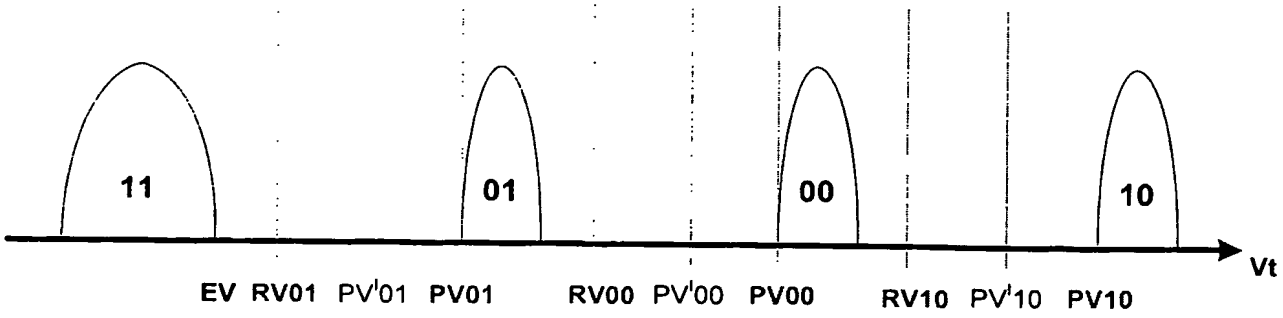

11
01
00
10
Vt
EV
RV01
PV'01
PV01
RV00
PV'00
PV00
RV10
PV'10
PV10

FIG 1B

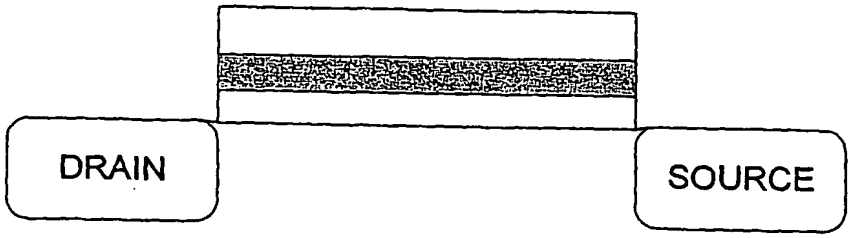
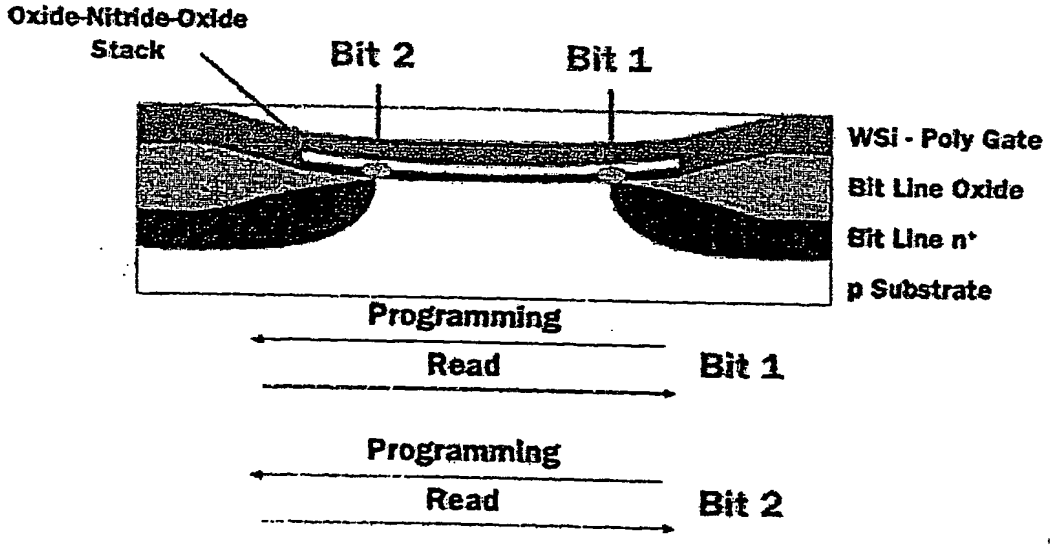


FIG. 2A

NROM Cell Structure



- 2 physically separated bits ⟶ The smallest bit size
- Program - CHE injection, Erase - HH injection
- Reverse Read

FIG. 2B

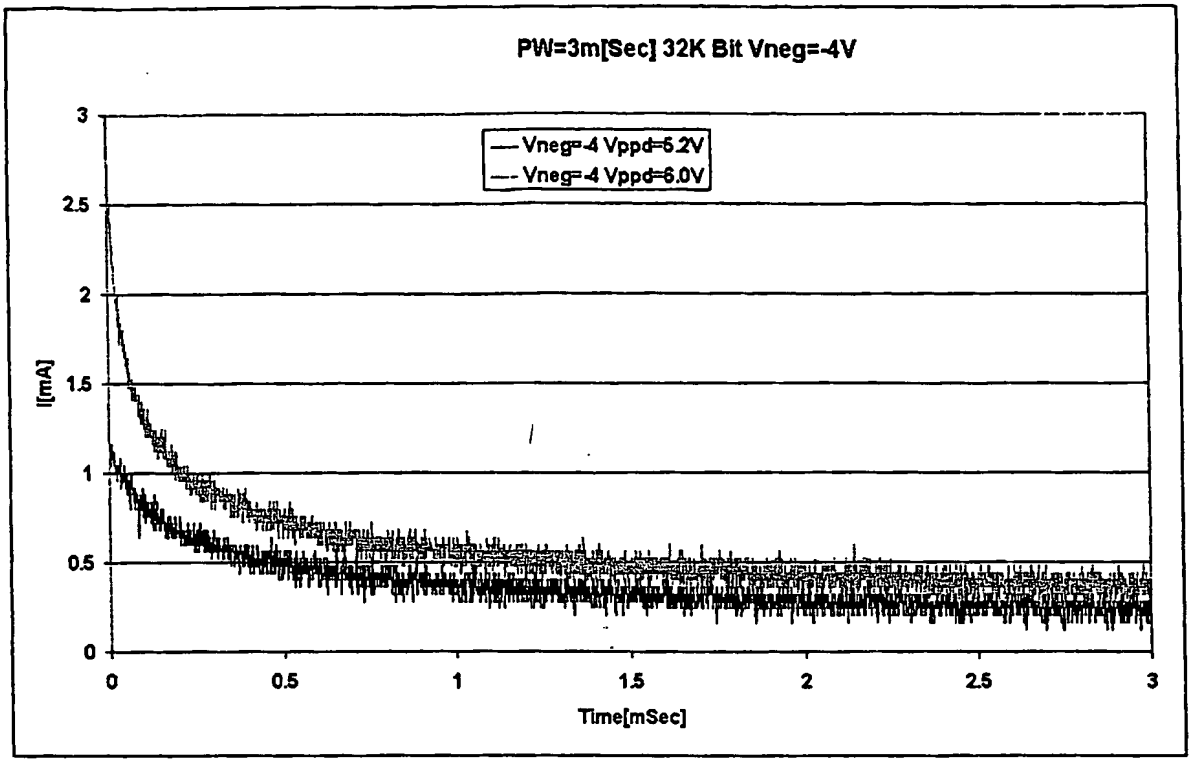

PW=3m[Sec] 32K Bit Vneg=-4V
Vneg=-4 Vppd=5.2V
Vneg=-4 Vppd=6.0V
I[mA]
Time[mSec]
0
0.5
1
1.5
2
2.5
3

FIG. 3

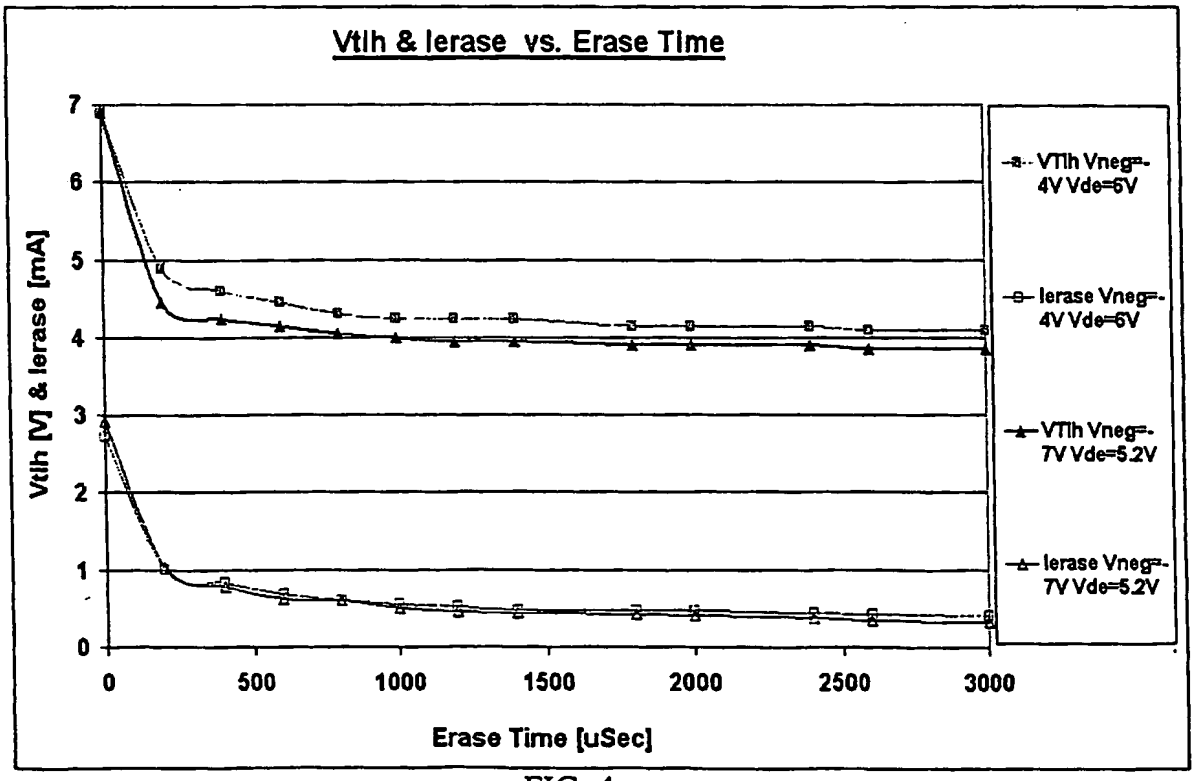

Vtlh & Ierase vs. Erase Time
Vtlh [V] & Ierase [mA]
Erase Time [uSec]
VTlh Vneg=-4V Vde=6V
Ierase Vneg=-4V Vde=6V
VTlh Vneg=-7V Vde=5.2V
Ierase Vneg=-7V Vde=5.2V
0
500
1000
1500
2000
2500
3000

FIG. 4

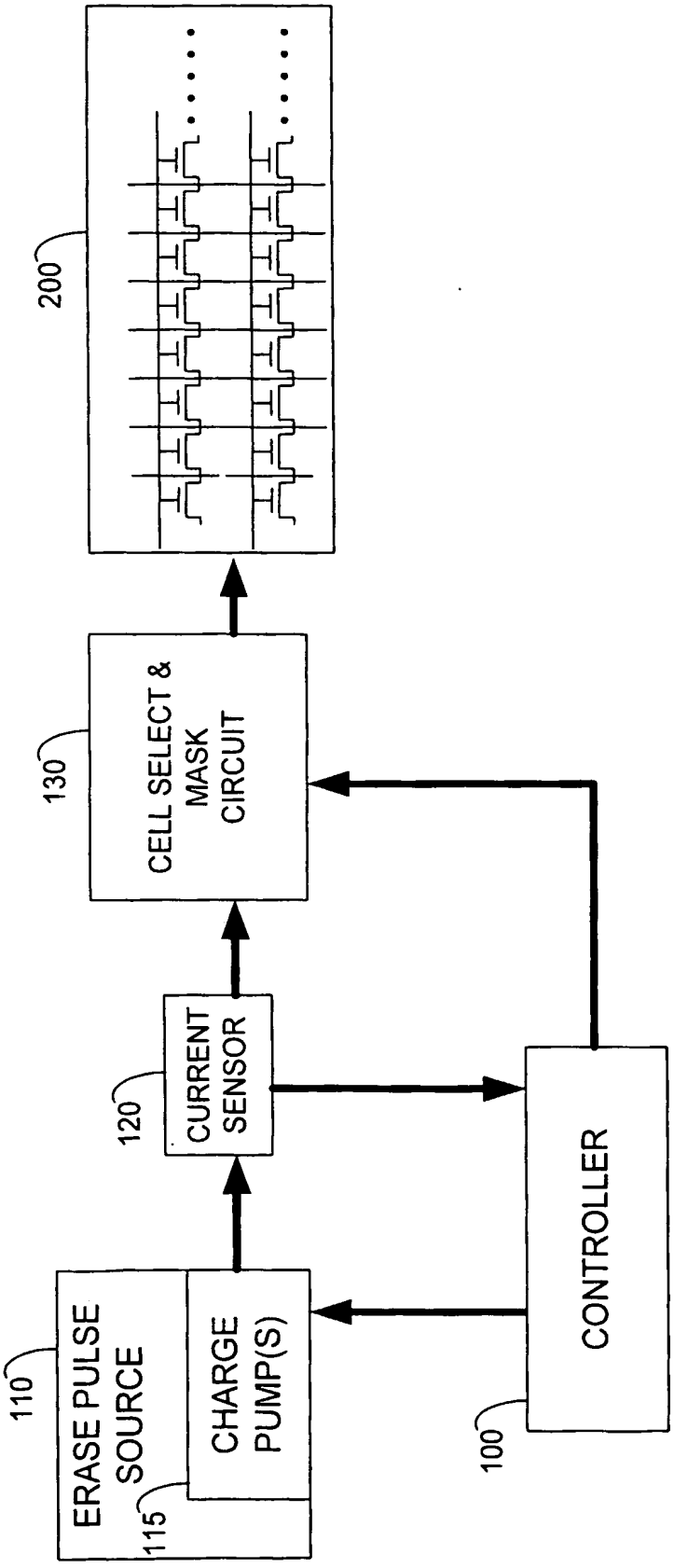

200
130
CELL SELECT & MASK CIRCUIT
120
CURRENT SENSOR
110
ERASE PULSE SOURCE
115
CHARGE PUMP(S)
100
CONTROLLER

FIG. 5

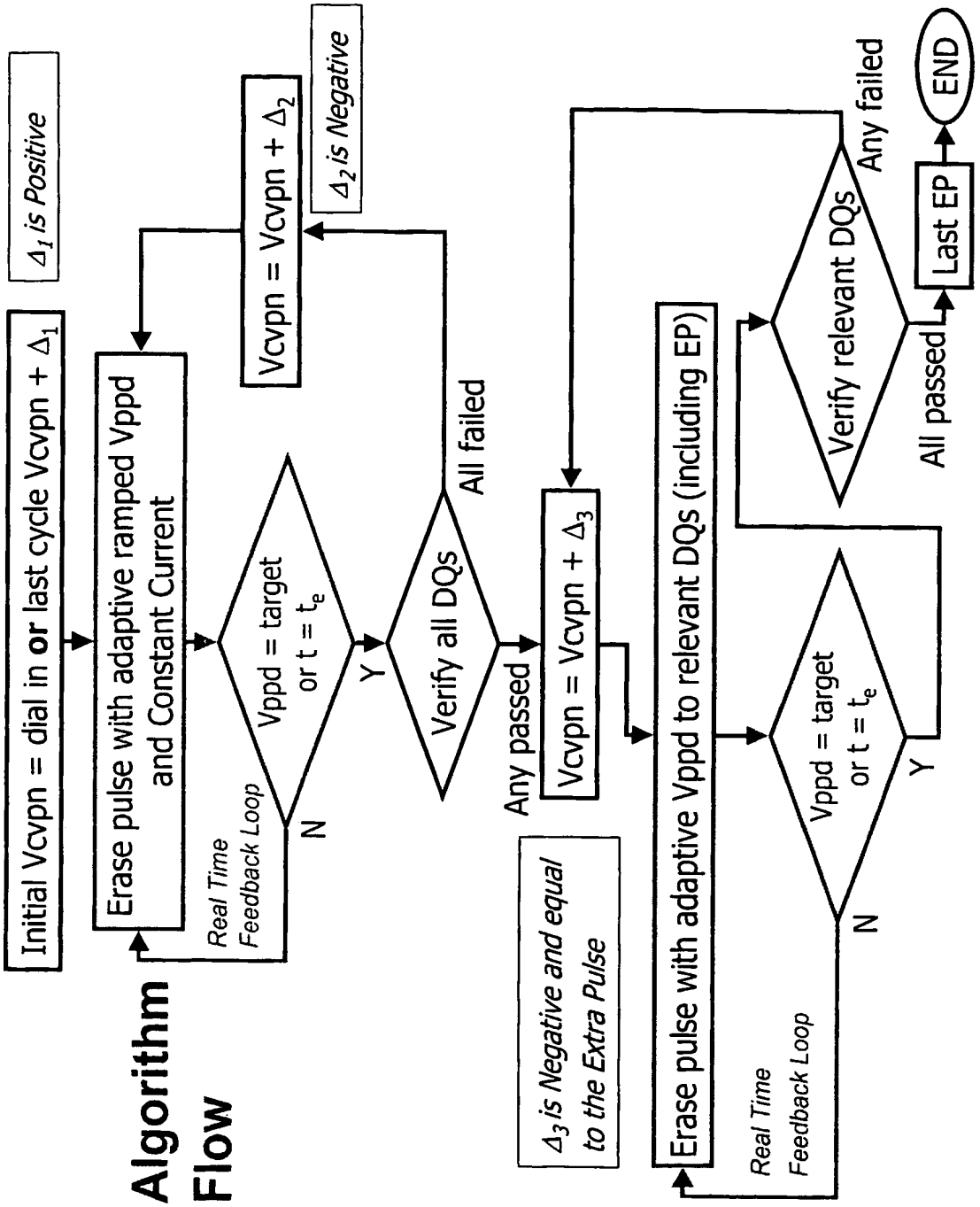

Algorithm Flow
Initial Vcvpn = dial in or last cycle Vcvpn + Δ1
Δ1 is Positive
Erase pulse with adaptive ramped Vppd and Constant Current
Real Time Feedback Loop
Vppd = target or t = te
N
Y
Vcvpn = Vcvpn + Δ2
Δ2 is Negative
Verify all DQs
All failed
Any passed
Vcvpn = Vcvpn + Δ3
Δ3 is Negative and equal to the Extra Pulse
Erase pulse with adaptive Vppd to relevant DQs (including EP)
Real Time Feedback Loop
Vppd = target or t = te
N
Y
Verify relevant DQs
Any failed
All passed
Last EP
END

FIG. 6

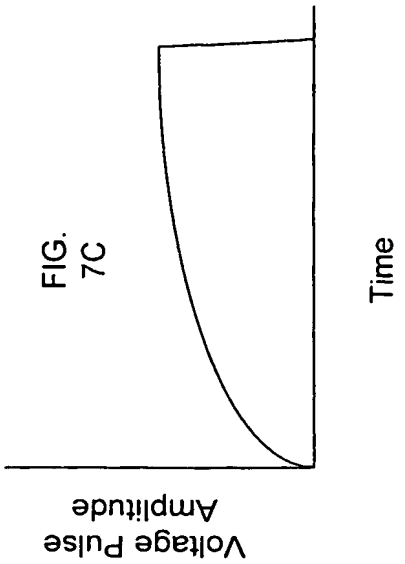


FIG. 7A
Voltage Pulse Amplitude
Time

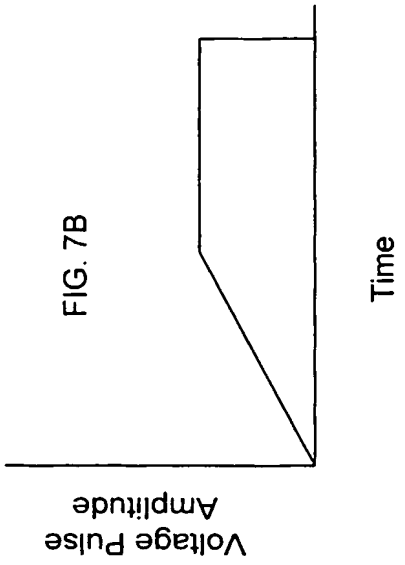


FIG. 7B
Voltage Pulse Amplitude
Time

FIG. 7C
Voltage Pulse Amplitude
Time

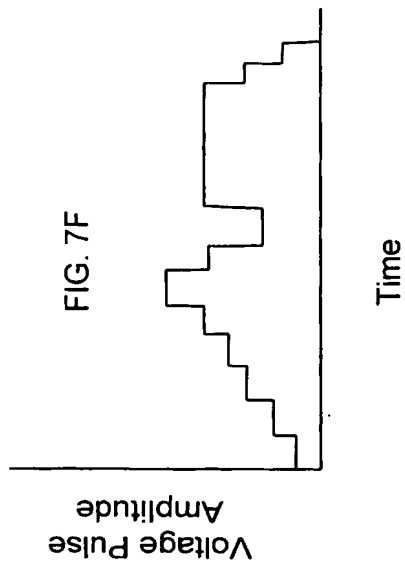


FIG. 7D
Voltage Pulse Amplitude
Time

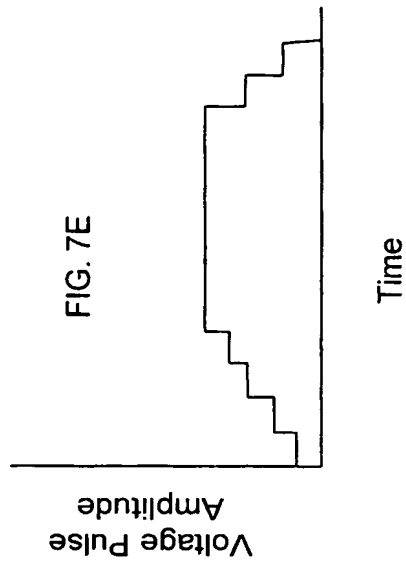


FIG. 7E
Voltage Pulse Amplitude
Time

FIG. 7F
Voltage Pulse Amplitude
Time

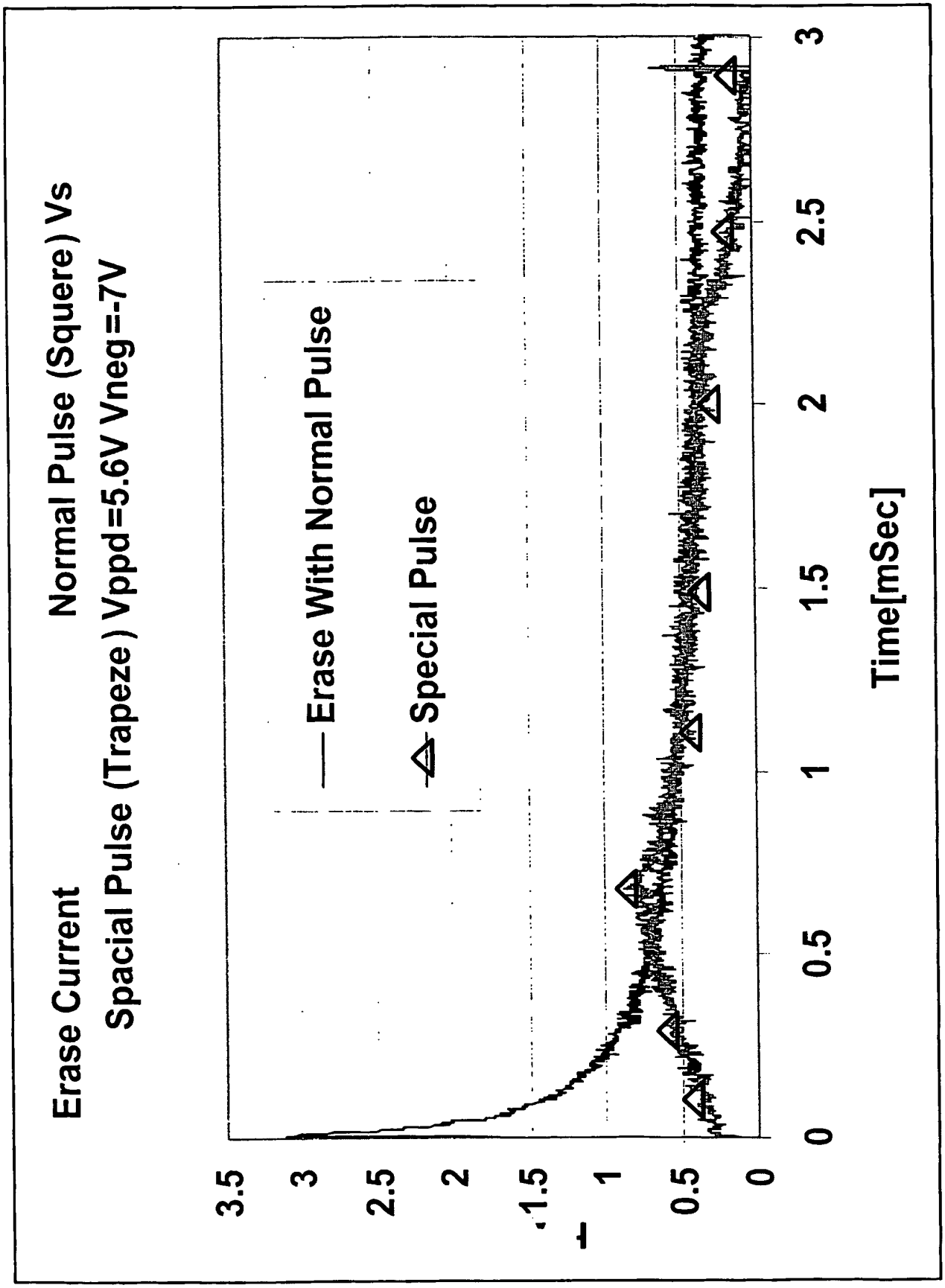

Erase Current
Spacial Pulse (Trapeze) Vppd=5.6V Vneg=-7V
Normal Pulse (Squere) Vs
Erase With Normal Pulse
Special Pulse
I
Time[mSec]
3.5
3
2.5
2
1.5
1
0.5
0
0
0.5
1
1.5
2
2.5
3

FIG. 8

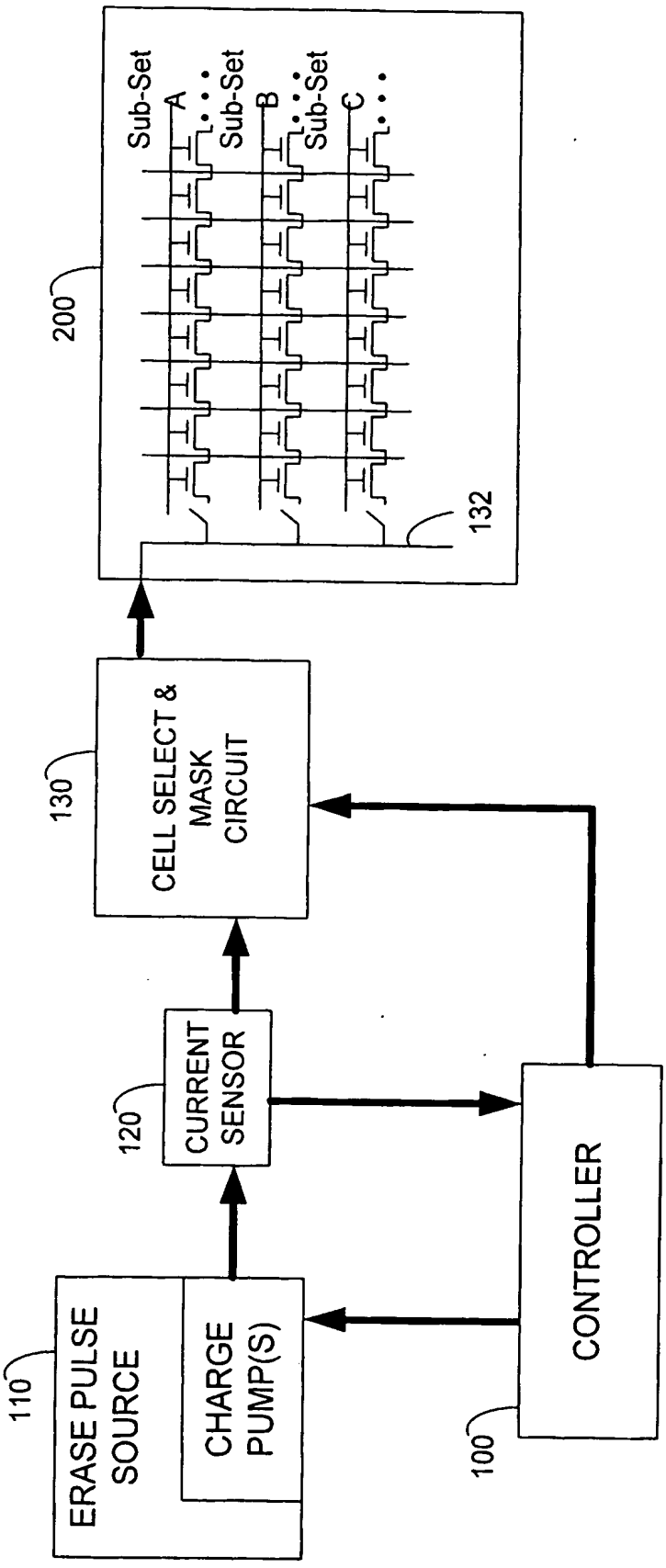

Sub-Set A
Sub-Set B
Sub-Set C
200
132
CELL SELECT & MASK CIRCUIT
130
CURRENT SENSOR
120
ERASE PULSE SOURCE
CHARGE PUMP(S)
110
CONTROLLER
100

FIG. 9

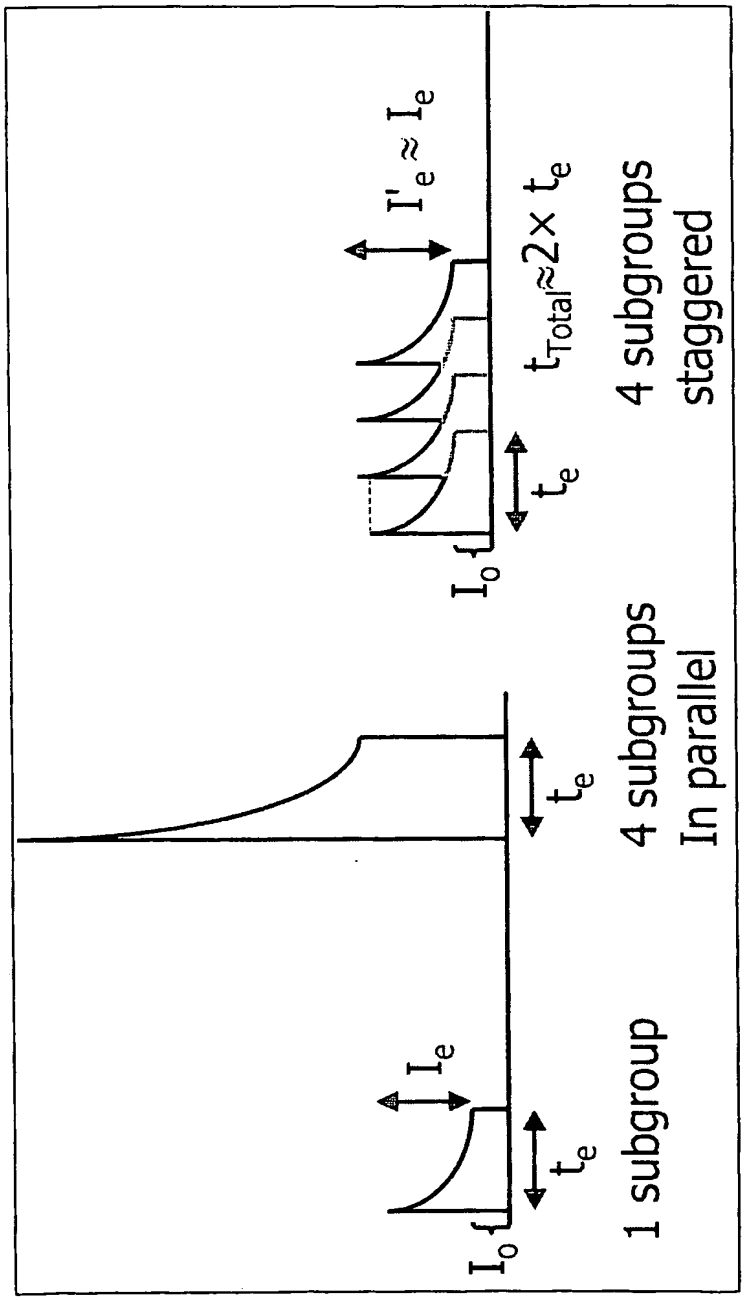

1 subgroup
I_e
t_e
I_o
4 subgroups
In parallel
t_e
4 subgroups
staggered
$I'_e \approx I_e$
$t_{Total} \approx 2 \times t_e$
t_e
I_o

FIG. 10